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Remarks

In view of the above amendments to the claims and the following discussion, the applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U. S. C. § 102. Thus, the applicants believe that all of these claims are in allowable form.

REJECTIONS

## A. 35 U. S. C. § 102

## 1. Claims 1-13 are not anticipated by Bu

Claims 1-13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bu (U.S. Patent Publication 2002/0101172 published August 1, 2002). The applicants submit that these claims are not anticipated by this reference.

The main amendments to claim 1 recite, that

- all of the emitters of each column *are* current supplied simultaneously through one single power supply line (ref. 4 on figs.1 & 2). *At the end of claim 1*, a representative value of the drain current supplying an emitter selected in a column is determined on the basis of the measurement of a representative value of the current flowing through the single power supply line of this column for supplying simultaneously all of the emitters of the column. See also same amendments in claims 3 and 4. The support for such amendments can be found at page 7, lines 33-34 and at page 10, lines 33-36.
- for each column of emitters, *there is only one single separate* unit for determining a representative value of the drain current supplying the selected emitter.
- Other amendments concern only a change of order of the features, that are proposed to improve the logic.

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Bu (US 2002/0101172), cited by the Examiner, is quoted in the application at page 12, lines 24-36 under the equivalent reference US 6,433,488: "To compensate for the trip-threshold voltages of the TFT transistors of an active matrix, it is known, for example from US document 6 433 488, to use an emitter drive circuit that includes a comparator capable of **comparing** the drain current  $I_d$  passing through the modulator with a reference current during a step of programming the drive circuit. However, this circuit requires the implantation of one switching unit (ref.5) per emitter in order to switch the supply source for the emitter between the programming step and an emission step of the emitter. This switching unit comprises two thin-film transistors and an inverting amplifier. This circuit is difficult to fabricate and is expensive." **Moreover, in Bu, two different power supply lines are needed for each column ("DRV" and "Vs" on fig.2), between which the switching unit (ref.5) operates.**

With regard to claim 1, Bu describes with respect to FIG. 2 (having similar elements as in FIG. 1) and paragraph 0016, at line 4, an active-matrix image display device comprising:

- several light emitters forming an array of emitters distributed in rows and columns (see, Bu at paragraph 0002 and paragraph 0016: "OLED array");
- power supply means (see, Bu at paragraph 22: "supply voltage Vs") capable of supplying current to emitters of a column during their emission steps, through a first current supply line of this column, and another "supply line Vpp" (see, Bu at paragraph 23 and "DRV" block of FIG. 3) capable of supplying a current DRV to successively each emitter of a column during their programming steps, through a second current supply line of this column;
- means for controlling the emission of the emitters comprising:
- for each emitter of the array, a current modulator (see, Bu at paragraph 6: transistor 21) comprising a source electrode ("current carrying electrode": 211 or 212), a drain electrode ("current carrying electrode": 212 or 211) and a gate electrode (213), a drain current being able to pass through said

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modulator in order to supply said emitter, for a voltage between the drain or the source and the gate equal to or greater than a trip-threshold voltage.

- for each modulator, storage means ("capacitor" 23) capable of storing electric charges at the gate electrode of the modulator; and
- for each row of emitters, row select means capable of selecting in succession the emitters of each row of emitters ("scan signal"; 3 – transistor 22), for programming these emitters, and
- for each column of emitters, column address means capable of addressing in succession each emitter of said column of emitters by applying, during the programming step of this selected emitter, a value representative of a data setpoint ("data signal") to the gate electrode of the modulator associated with this emitter (see, Bu at paragraph 0007),
- trip-threshold voltage compensation means comprising comparators, the comparators being capable of comparing, during the step of programming a selected emitter, a value representative of the drain current supplying the selected emitter with the value representative of the data setpoint for controlling the quantity of charge stored in the storage means.

Bu does not disclose:

- a) for each column, a single current supply line to supply current to all emitters of this column, whatever these emitters are on programming steps or on emission steps (see, Bu at FIG. 1, the switching unit 5 provides a first current supply line to supply "DRV" current, and a second supply line to supply the voltage "Vs" for the emission steps);
- b) one single separate determination unit for each column of emitters, adapted to determine the representative value of the drain current supplying the emitter selected in a column on the basis of the measurement of a representative value of the current flowing through the single power supply line of this column for supplying simultaneously all of the emitters of this column. More specifically, in Bu, even if there would be one single separate determination unit for each column of emitters, this determination unit would be actually capable of

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determining a value representative of the drain current supplying an emitter selected in this column, BUT on the basis of a measurement of a representative value of the current flowing through the **second** (see above) current supply line "DRV" of this column for supplying **successively** (i.e. according to the "scan signal" actuating the switching means 5) **each** of the emitters of this column (differences are in bold characters). Consequently, claim 1 is not described in Bu.

In view of the above arguments, Applicants respectfully submit that claim 1 is patentable over Bu and therefore, claims 2-13 are also patentable based on their dependence upon claim 1.

### CONCLUSION

Thus, the applicants submit that none of the claims, presently in the application, are anticipated under the provisions of 35 U. S. C. § 102. Consequently, the applicants believe that all of the claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

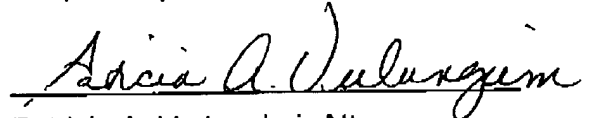
If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application,

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it is requested that the Examiner telephone Ms. Patricia A. Verlangieri, at (609) 734-6867, so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,



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